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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,179	09/15/2003	Gheorghe C. Cascaval	YOR920030127	9439
34663 7590 01/10/2007 MICHAEL J. BUCHENHORNER 8540 S.W. 83 STREET MIAMI, FL 33143			EXAMINER PAN, DANIEL H	
			ART UNIT	PAPER NUMBER
			2183	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		01/10/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/662,179	Applicant(s) CASCAVAL ET AL.	
	Examiner Daniel Pan	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 4-15 is/are pending in the application.
 4a) Of the above claim(s) 2 and 3 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 4-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

1. Claims 1, 4-15 remain for examination. Claims 2,3 have been canceled.
2. Alferness et al. (5,577,259) has been introduced in response to applicant's amendment in claim 1. However, rejections set forth in previous action have been maintained and the response to applicant's remarks will follow.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Alferness et al. (5,577,259).

1. As to claim 1, Alferness taught at least :
 - a) an indirection table (see fig.16 [0-0777]) comprising a plurality of entries for encoding register patterns , each register pattern identifying a register tuple (see the micro address of multiple entries in col.15, lines 48-55);
 - b) instructions for loading and storing entries in the indirection table (see the micro code instruction of a micro program for each extended mode instruction in col.15, lines 48-55);

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- c) a mechanism for identifying instructions that use the indirection table (see the 10 bit vector address bit in col.15, lines 43-47); and
- d) a mechanism for identifying a set of bits in instructions that are used to index into the indirection table (see the index value [168] in fig.17, col.20, lines 26-41);
- e) a plurality of registers (see the memory RAM 148) identified by a register pattern (see fig.16 address map);
- f) compatible mode for interpreting register directly (see basic mode in col.15, lines 55-67), and extended mode for interpreting the register access fields via the indirection table (see the extended mode in col.15, lines 48-55).

The following rejections have been maintained and incorporated by reference the last Office action on 05/15/06.

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

- 2. Claims 1- 15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.
- 3. See response to applicant's remarks in this action.
- 4. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Devic (6,072,508).
- 5. As to the newly amended claim 1, Devic also taught at least :

6. a) compatible mode for interpreting register access field directly (see col.2, lines 18-43, see the operand register fields), and extended mode for interpreting the register access fields via the indirection table (see fig.3B 240).

7. The response filed on 10/18/06 has been fully considered but it is not persuasive.

In the remarks, applicant argued that :

a) Devic does not encode or decode the registers;

b) Devic does not teach identifying an entry in a table, the entry comprises a plurality of identifiers;

c) lookup table of Devic included offsets, not register identifiers;

d) a CPU with an increased number of registers has improved processing power.

8. As to a) above, Devic taught a lookup table of the display list (see col.7, lines 9-35. See also the display list for a compatible mode for interpreting register access field directly in col.2, lines 18-43 and the extended mode for interpreting the register access fields via the indirection table fig.3B 240). Therefore, the lookup table itself was a decoder.

9. As to b), c) above, Devic's offsets did identify one of the partitions of the registers in register file 112 (see fig.3B). Therefore, each bit of the offset was an identifier of a register in a partition (64netries distributed with 1024 registers). Devic also had identifying an entry [offset] in a table [240], the entry comprises a plurality of identifiers (6 offset bits, see col.8, lines 14-21), see reference to the table 240 in col.7 , lines 19-22 for identifying the entry).

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10. As to d), a CPU with an increased number of registers has improved processing power is an intended use. No details of the CPU component with the registers have been recited into the claim.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. All references were cited in the previous action.

a) Gaither et al. (4,453,212) is cited for the teaching of index into a table with register pattern (see fig.1 and fig.2, col.3, lines 35-67, col.4, lines 1-5);

b) Tanahashi (4,466,056) is cited for the teaching of the index by the instruction bits into a table (see col.5, lines 65-68, col.6, lines 1-53);

c) Kaplinsky (4,361,868) is cited for the teaching of 2^B with the extended register specifiers (see fig.3, col.6, lines 27-68, col.7, lines 1-23).

Applicant's amendment (claim 1) necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


DANIEL A. PINI
TECHNICAL EXAMINER
USPTO